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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,800	04/27/2001	Takashi Nakamura	206608US2	2801

22850 7590 07/19/2004

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EXAMINER	
WU, XIAO MIN	

ART UNIT	PAPER NUMBER
2674	5

DATE MAILED: 07/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/842,800	Applicant(s) NAKAMURA ET AL.	
	Examiner XIAO M. WU	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 25-30 and 35-37 is/are allowed.

6)☒ Claim(s) 1-6,10-12,18,19, 24 and 31-34 is/are rejected.

7)☒ Claim(s) 7-9,13-17 and 20-23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5, 10, 31-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "the valid digital pixel data" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 31 recites the limitation "the inputted operation mode" in 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 32 recites the limitation "said operation" and "the valid bits" in line 2 and line 3, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim 33 recites the limitation "the inputted operation mode indication signal" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim 34 recites the limitation "said operation mode" in line 2. There is insufficient antecedent basis for this limitation in the claim.

The recitation of "whose number is equal to 1/N of the total number of the signal lines", in claim 10, lines 4-5, is not understandable because the latch circuits must be greater than 2. However, the number "1/N" is less than 1.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US Patent No. 5,856,818) in view of Ueda et al. (US Patent No. 5,739,887).

As to claims 1, 4, Oh discloses a display apparatus comprising: signal lines (e.g. output lines of source IC 14, 15 of Fig. 1) scanning lines (e.g. output lines of the gate IC 13) arranged laterally and longitudinally; display elements (16) formed respectively points of intersection of the signal lines and the scanning lines; a signal line driving circuit (14, 15) configured to drive the signal lines, a scanning line driving circuit (13) configured to drive the scanning lines; a graphic controller IC (11, Fig. 1, also see col. 1, lines 49) configured to outputs digital pixel data in order according to the order f driving the signal lines by the signal line driving circuit; wherein

the graphic controller IC outputs a clock signal in a cycle twice as much as that of the digital pixel data (e.g. 2CLK has a cycle twice as much as that of the digital pixel data, see Fig. 18), and the signal line driving circuit and the scanning line driving circuit drive the signals and the scanning lines synchronously with the signal, respectively (see Fig. 8A).

It is noted that Oh does not specifically discloses that the signal and scanning line driving circuits are formed on the insulating substrate. Ueda is cited to teach a LCD device including gate driver and data driver formed on the insulated substrate (see Fig. 3). It would have been obvious to one of ordinary skill in the art to have modified Oh with the features of the driving circuit formed on the same substrate with the LCD because the driver ICs as chip-on-glass packaged on the two sides of the liquid crystal display panel usually on the longer two sides, are driven in parallel by the two display controllers thereby to improve the temperature resistance and to take an advantage in compactness (col. 7, lines 24-28).

As to claim 2, Ueda discloses the controller IC is mounted on the insulating substrate (see Fig. 3).

As to claim 12, note the discussion of claim 1 above, Oh further discloses an order control circuit (33, Fig. 23, Fig. 3), and in a dual bank data driver, both color signals of even number and odd number from the timing controller are inputted simultaneously to upper data driver ICs and lower data driver ICs. Therefore, in the dual bank data driver, the upper data driver ICs and the lower data driver ICs simultaneously drive every source lines of the LCD panel (col. 2, lines 24-31). Ueda further discloses a plurality of data busses arranged from substantially the center of one side of the insulating substrate toward both the ends of the side (e.g. the controller 101 unit 101 is located on the center of one side of the insulate ting substrate.

4. Claims 3, 6, 11, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US Patent No. 5,856,818) in view of Ueda et al. (US Patent No. 5,739,887) as applied to claims 1-2 and 4 above, and further in view of Okumura et al. (.US Patent No. 6,344,850).

As to claim 3, 6, 11, 24, it is noted both Oh and Ueda does not disclose the graphic controller IC has a phase adjusting circuit configured to adjust the phase of the digital pixel data and tat of the clock signal. Okumura is cited to teach a phase adjusting circuit (5) for adjusting the phase of the pixel data and that of the clock signal. It would have been obvious to one of ordinary skill in the art to have modified Oh as modified with the feature of the phase adjusting circuit as taught by Okumura because in Okumura's device, the number of transition times of the logic state of the differential data can be greatly reduced by a appropriately choosing the delay period (col. 2, lines 4-6).

As to claim 6, Okumura further discloses a polysilicon TFT.

5. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable Okumura et al. (US Patent No. 5,945,972) in view of Quanrud (US Patent No. 6,339,417).

As to claim 18, Okumura discloses display apparatus comprising: a memory cell (121a, .., 121m, Fig. 5) comprising a plurality of memories arranged laterally and longitudinally; a display layer (110, Fig. 2B) in which display can be variably controlled according to the values of the plurality of memories; a writing control circuit (124, Fig. 3) configured to control the writing operation to the memory cell; an order control circuit (123) configured to control the order of digital pixel data to be transmitted on the data busses to the memories are simultaneously driven every plural memories by the writing control circuit. It is noted that Okumura does not discloses

that the memory is a 1-bit memory and a plurality of data busses arranged from substantially the center of one side of the insulating substrate.

Quanrud is cited to teach a display system having multiple memory elements per pixel similar to Okumura and one bit memory can be used in Quanrud (col. 12, lines 56-58). It would have been obvious to one of ordinary skill in the art to have modified Okumura with the feature of the one bit memory as taught by Quanrud because number of the bits used for the data can be choose for different resolution. Ueda further discloses a plurality of data busses arranged from substantially the center of one side of the insulating substrate toward both the ends of the side (e.g. the controller 101 unit 101 is located on the center of one side of the insulating substrate. It would have been obvious to one of ordinary skill in the art to have modified Okumura as modified with the controller located on center of one side of the substrate as taught by Ueda because Ueda provides an compact design for a display.

As to claim 19, Quanrud discloses that the memories are sued to store color data.

Allowable Subject Matter

6. Claims 25-30, 35-37 are allowed.

7. Claims 7-9, 13-17, 20-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The US Patents 5,170158, 6,072,456, 6,307,531, 6,462,725, 6,664,943 are cited to teach a LCD driving circuit.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiao Wu whose telephone number is (703) 305-4721.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377

xw

July 11, 2004

XIAO WU
PRIMARY EXAMINER
ART UNIT 2674